Interconnection Networks
ECE 8823A / CS 8803 – ICN
Spring 2016
Monday & Wednesday, 3:05 – 4:25 pm, Klaus 1447

Prerequisite(s): ECE 6100 / CS6290, or equivalent
Instructor: Tushar Krishna (tushar@ece.gatech.edu)

Course Objectives
Interconnection Networks refer to the communication fabric interconnecting various components of a computer system. They occur at various scales – from on-chip networks (OCN)/Networks-on-Chip (NoCs) in billion-transistor many-core chips, to custom high-speed wired networks in supercomputers, to optical fiber networks within datacenters. The growing emphasis on parallelism, distributed computing, and energy-efficiency across all these systems makes the design of the communication fabric critical to both high-performance and low power consumption. This course examines the architecture, design methodology, and trade-offs of interconnection networks. The material covered in this course bridges the gap between disciplines/courses such as VLSI interconnects, digital communication, computer architecture, distributed systems, and computer networks. The overall focus of the course will be on interconnection network architectures used in multiprocessor and many-core systems, and designing for the communication requirements of various parallel architectures and cache coherence mechanisms.

In the first half of the course, lectures will cover the fundamentals of interconnection networks, getting to the research frontier at each level – topology, routing, flow-control, microarchitecture, network interfaces, and system interactions. The second half of the course will focus on state-of-the-art research and case studies, using a mix of lectures, student presentations, paper readings, discussions, and debates on contrasting approaches. Towards the end, opportunities for interconnection networks in the presence of emerging trends such as heterogeneous systems and the Internet-of-Things will be explored.

At the end of this course, students will be able to appreciate both the architectural and the physical design nuances/trade-offs involved at each level of an interconnection network. They will acquire the skill sets to design state-of-the-art networks for multicore processors from industry leaders like Intel, AMD, IBM, Qualcomm, and so on. Students will also be able to summarize and critique research papers on Interconnections Networks / Networks-on-Chip from leading conferences and journals. The course projects will focus on solving open-ended research problems and can lead to publications in reputed journals/conferences/workshops. Projects aligned with both the students’ own graduate research and the course will also be encouraged.

Course Text
The material for this course will be derived from the following texts:

4. Papers from recent conferences: ISCA, MICRO, HPCA, ASPLOS, NOCS, DATE, DAC, ICCAD, ICCD, ISSCC
Syllabus and Outline

1. Introduction to Interconnection Networks
   - Introduction
   - Types of Networks
   - Evaluation Metrics

2. Topology
   - Metrics for comparing topologies
   - Direct Topologies
   - Indirect Topologies
   - Hierarchical Topologies

3. Routing
   - Deterministic Routing
   - Oblivious Routing
   - Adaptive Routing
   - Deadlock Avoidance

4. Flow-Control
   - Message-based Flow Control
   - Packet-based Flow Control
   - Flit-based Flow Control
   - Virtual Channels
   - Deadlock Avoidance

5. Microarchitecture
   - Router Organization
   - Pipeline
   - Optimizations
   - Buffer Management
   - Crossbar Design
   - Allocators and Arbiters

6. System Interface
   - Shared Memory Multiprocessors
   - Cache Coherence
   - Deadlocks
   - Message Passing

7. Implementation: RTL and Circuits
   - Wire Delay
   - Router Pipelines
   - Power Consumption
   - Area Overheads

8. Advanced Topics
   - Physical and Virtual Express Topologies
   - Single-cycle Multi-hop Networks
   - Multicast Communication
   - Silicon Photonics
   - Reliability and Faults
   - GPU Networks
9. System-level Networks
   - Supercomputers
   - Clusters
   - Datacenters

10. Case Studies with Real Chips
    - Intel SCC
    - ST Spidergon
    - Tilera TILE64
    - UT Austin TRIPS
    - MIT Broadcast NoC
    - University of Michigan Swizzle Switch
    - D E Shaw Research Anton 2
    - IBM BlueGene Q

11. Emerging Trends
    - Heterogeneous Systems
    - Mobile Communication / Internet-of-Things

Course Grading

<table>
<thead>
<tr>
<th>Component</th>
<th>Weight</th>
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<tbody>
<tr>
<td>Lab Assignments</td>
<td>10%</td>
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<tr>
<td>Midterm</td>
<td>25%</td>
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<tr>
<td>Paper Reviews</td>
<td>10%</td>
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<tr>
<td>Presentation on Paper/Case Study</td>
<td>10%</td>
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<tr>
<td>Class Participation and Pop Quizzes</td>
<td>10%</td>
</tr>
<tr>
<td>Project</td>
<td>35%</td>
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The early part of the course will cover fundamentals of interconnection networks (topology, routing, flow-control, and microarchitecture). The midterm will test knowledge of this theory. The remainder of the course will follow a research format involving paper readings, discussions and presentations. The assignments will introduce the students to Network-on-Chip simulator Garnet (distributed within the gem5 (www.gem5.org) open source full-system multi-core simulator). The research project will cover research problems in modern network design. Students will study relevant papers, propose a solution, implement the solution (via simulation) document the project (short paper) and present the paper in a conference format (20 minutes).

Course Policies

If you have a documented emergency or a university mandated reason because of which you have to miss an exam, get in touch with the instructor before (preferable) or latest by the day of the exam.

Learning Accommodations

If needed, we will make classroom accommodations for students with disabilities. These accommodations should be arranged in advance and in accordance with the office of Disability Services (http://www.adapts.gatech.edu)